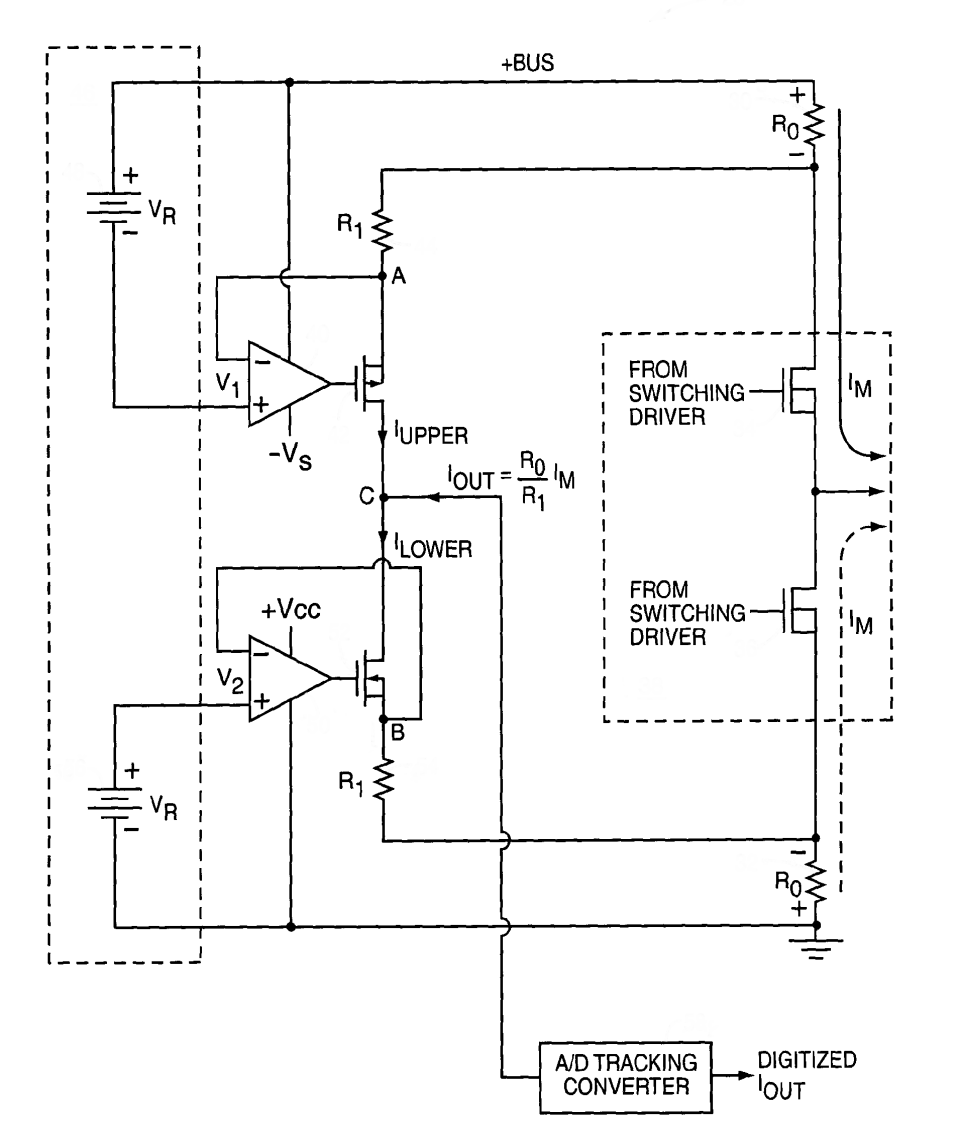
New High Performance Current Sense Circuit for DC Powered Three Phase Servo Controller

Donald E. Fulton
Consulting Engineer

US Patent 6,998,800, Feb 14, 2006

Idealized Current Sense – One Phase



- **Function**
  - Outputs continuous A/D tracking current
  - Iout = (R0 x Imotor)/R1 = (R0/R1) x Imotor
  - Current Ratio 1/50,000 (typ)
- **Implementation**
  - Two sense R's per current
  - R's embedded in op amp/FET current sources
  - Level shift & summation in one step
- **Advantages**
  - Designed for 3 phase DC powered servo
  - High performance, high BW
  - Inexpensive, surface mount compatible
  - Stable offset
  - Accurate gain
- **Caveats/Limitations**
  - No isolation
  - Designed for A/D & Inverter with common gnd
  - Designed for 20 VDC to 90 VDC bus
  - Usable to 180 VDC bus (maybe higher)
- **Status**
  - In production since 2003

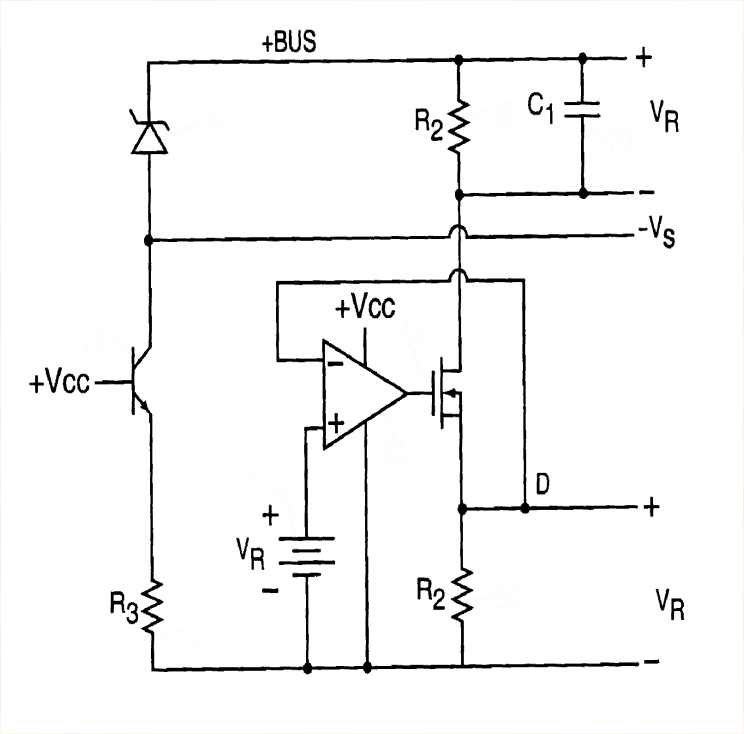
Design Challenges (Idealized => Practical)

- **Stabilize output offset**
  - **Major goal is very stable offset**
    - Objective is to ***permanently*** null offset during drive manufacture
  - **Idealized circuit has two *independent* references that both need to be stable**
  - **Design challenge is to eliminate the need for stable references**

- **Filters**
  - **RC's to prevent switching noise from affecting current sources**
    - In early testing the offset was found to be dynamically unstable
    - Dynamic offset instability was traced to burst of 10 mhz ringing for 500 nsec after each switching transition that briefly saturated the upper current source FET
  - **RC's to help translate output current from power gnd to A/D logic gnd**

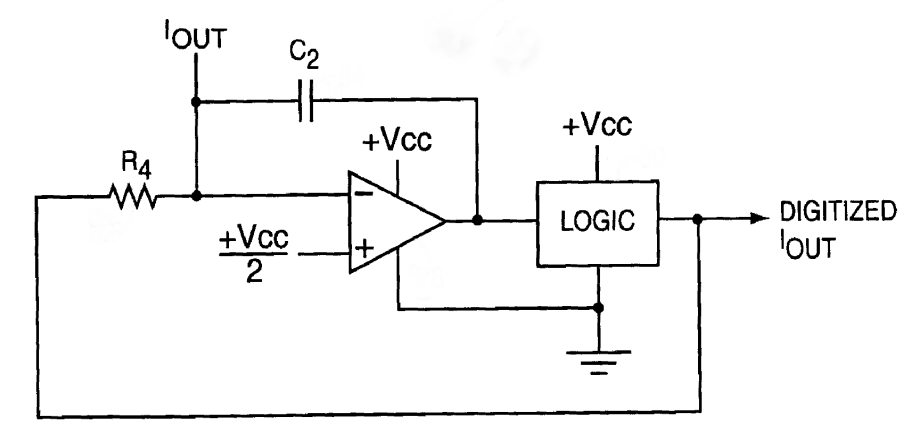
- **Sensing two currents**
  - **In idealized circuit references connect to +bus & gnd at Kelvin terminals of sense resistors**
    - It is not obvious where to connect one set of references if there are two currents to sense with four sense resistors
    - Does sensing two currents mean twice the parts?
  - **Design challenge is how to simplify a two current sense circuit**
    - Is there a way to share one set of references?

Improved References



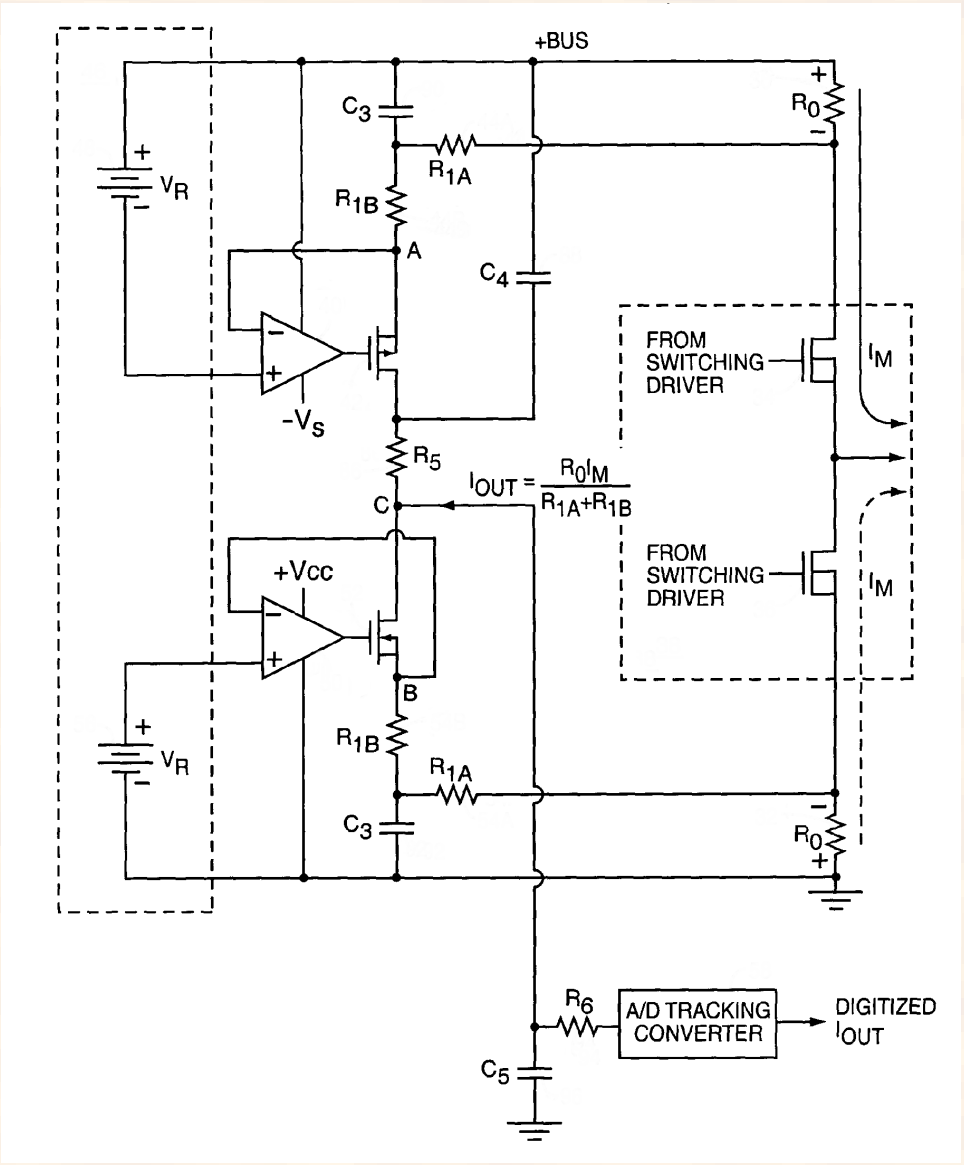
- **Idealized Circuit has an architectural weakness**
  - Upper and lower current sources have their bias currents set by *independent* references. The drift of both references contribute to drift in output offset current. Hence, for stable output offset in the idealized circuit *two* stable references are required.
- **Biasing upper and lower current sources from a single reference**
  - One external reference (Vr) biases a fixed current source with R2 source resistor and loaded by R2. This creates an upper reference hung from the +bus that is *slaved* to the lower ground based reference.
    - Upper reference impedance of R2 is not a problem because load on the upper reference is very light
  - Drift of the external reference (Vr) causes the magnitude of the upper and lower current sources to *drift up and down together,* hence output difference current to the A/D is largely unaffected
    - *S*tability of output offset is desensitized to drift of the single, external, reference by typically *two orders of magnitude*
    - Offset is stable even if Vr is *not* stable
- **Power for upper circuitry is provided by simple fixed current bleed with zener regulation**
  - Few ma of current bled from the +bus through a zener by an NPN current source is adequate to power a rail-rail CMOS op amp for the upper current source(s)

Tracking A/D Converter & Grounding



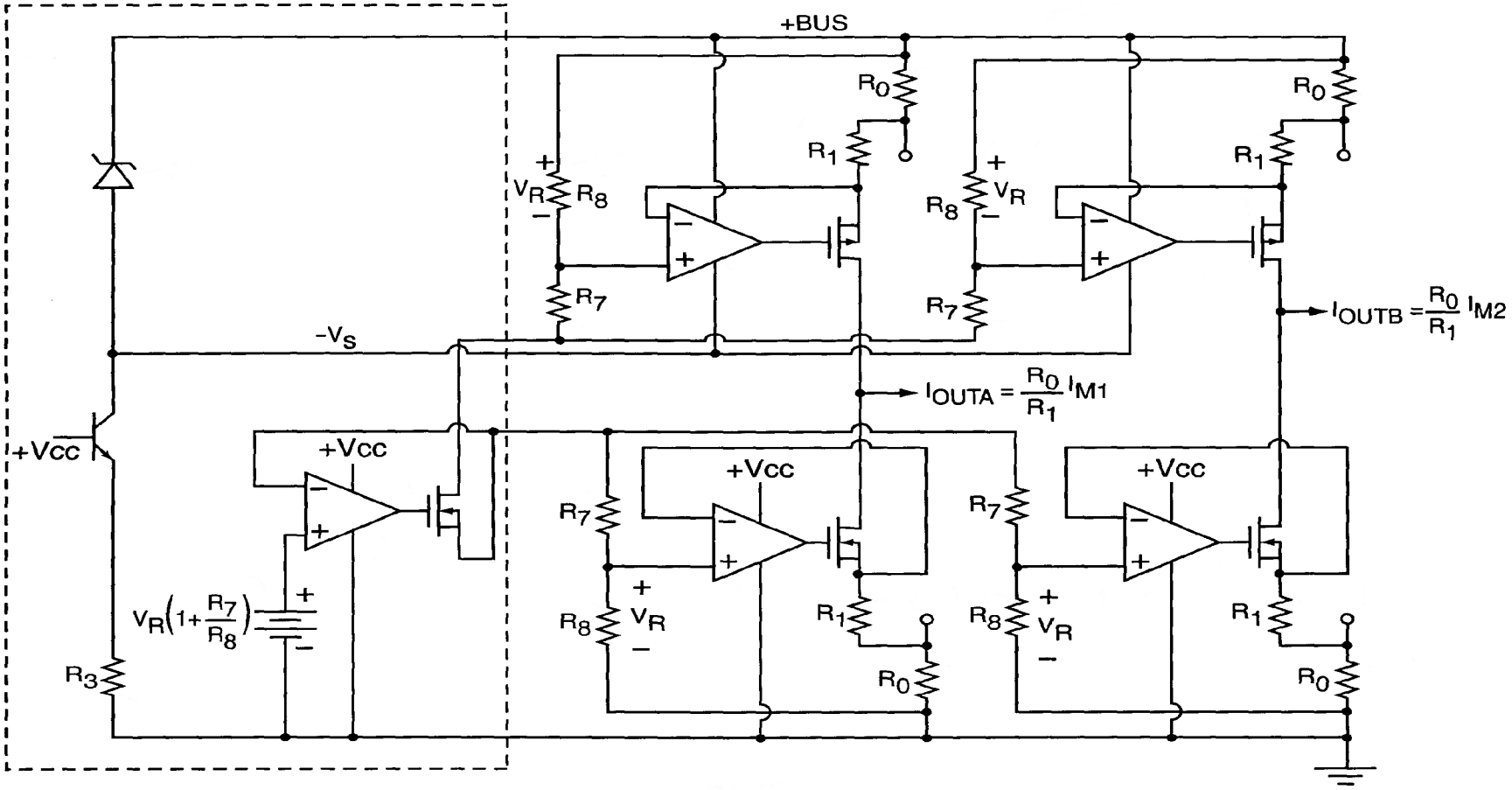
- **A/D's bias voltage (Vcc/2) does two jobs**
  - Biases A/D for +/- current
  - Biases lower current source into linear region
    - Current sources ***must*** operate in linear region at ***all times***
- ***A/D's logic gnd is tied to inverter/power gnd***
  - Logic and power gnds typically are connected at a single point
  - Logic gnd plane was tied to power gnd at the lower sense resistors common terminal
  - Current sense high output impedance and properly placed A/D input RC was effective in keeping gnd noise out of the A/D input

Adding Filters



- **Filtering Sense R's output voltage**
  - Split R1 and add C3
  - RC = 0.5 usec to 1 usec (typ)
- **Protecting current source FET's from power stage noise**
  - C4 & C5 with R5 keep FET's in linear region at all times ***(Important)***
- **Current sources should be layed out tightly**
  - Great care should be taken in the placement of filter caps since they need to be effective at high frequencies
  - Ceramic capacitors work well. C4 may need to be a high voltage ceramic.
- **Overall Iout response time**
  - 1.5 usec to 2 usec (typ)

Complete Two Phase Current Sense Circuit



- **Two phases sharing a reference**
  - Quasi-floating local references are created by dividing common references with R7,R8 divider at each current source {R8/(R7+R8) =1/6 typ}
  - Sense resistor (Ro) pairs are layed out adjacent to minimize CM voltage between them