Current Sense Circuit for a DC Powered Three Phase Servo Motor Controller

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***Abstract* - This paper presents a new, high performance, inexpensive, current sense circuit that outputs signal currents that continuously track motor currents in a three phase servo motor. Each tracked motor current uses two current sense resistors, one connected to +bus and the other to ground, which are embedded in opposed op amp-mosFET current sources that provide level shifting and summation. The offset and gain of the circuit are very stable. This circuit has no isolation as it is designed to be used with a DC powered motor controller that shares a common ground with the controlling electronics.**

I. Introduction

A. Compatibility Requirement

The current sense circuit to be discussed in this paper was designed to provide current feedback for a three phase PM servo motor (25A) controlled by a DC powered drive (20V to 90V bus). The current sense circuit has no isolation because it is designed to be used with a DC powered motor controller that shared a common ground with the controlling electronics. The DC servo drive was developed as a member of a next generation family of servo drives that was to include both offline AC drives and isolated DC drives. All of the drives in the family, AC and DC, were to have state-of-the-art performance with similar specs and to be controlled by the same digital control electronics. The AC drives of the family were to use current sensors in series with the motor leads that provided high quality, continuous, fast, current sensing, so the DC servo drives needed to have current feedback of similar quality or better. The usual approach to sensing current in a three phase DC drive is to put sense resistors only in the ground sides of the bridge legs and to sample the outputs. Several such bottom sampling algorithms have been patented. To meet the family control commonality goals it was decided that the DC drive needed to have continuous, not sampled, current feedback, and to meet the performance specs it was necessary that the offset and gain be very stable over time and temperature.

II. Concept

A. Placement of Sense Resistors

It follows directly from Kirchhoff"s laws that, in principle, one can replace a single sense resistor in a bridge leg output with two sense resistors, one at the top connected to +bus, and a second at the bottom connected to ground, whose outputs can be summed (with the correct polarity) to provide a signal that continuously monitors one motor current.

B. Design Challenge

The design challenge, of course, is to level shift the small upper sense voltage down from near +bus to near ground without degrading it. Many level shift circuits exist and have been used for decades, but the simple ones typically add a substantial, temperature sensitive offset term into the signal and/or they degrade the gain with a (1-1/beta) gain term. The level shifting in the circuit of this paper is free of such errors. This circuit converts the small sense voltages from the top and bottom sense resistors directly to currents by embedding the sense resistors in the source legs of op amp-mosFET current sources, as shown in Fig 1. By opposing the current source outputs the required level shifting and summation are performed in one step.

III. Principle of Operation

A. Idealized Circuit

Fig 1 is an idealized circuit showing the sensing of one motor current. It will be used to describe the principles of operation of the new current sensor.

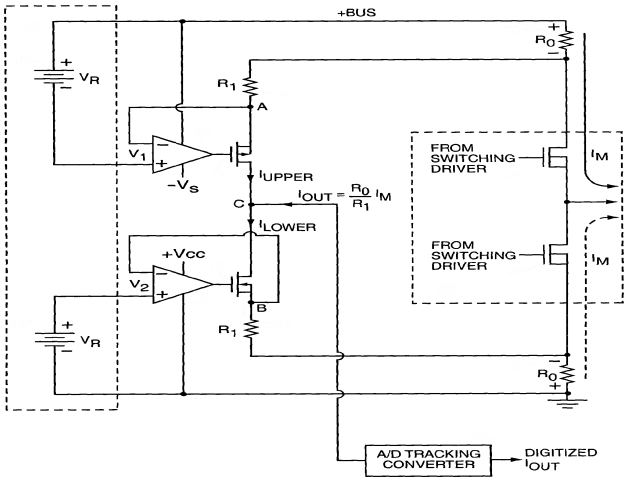

Figure 1. Idealized Current Sense Circuit

1 senior power engineer at Kollmorgen (Danaher Motion) during the development of this circuit

One sense resistor is placed between the +bus and upper power transistor. A second similar sense resistor is placed between ground and the lower power transistor. The sense resistors would typically be a few mohm with output voltages in the 100 mv to 150 mv range at full motor current.

B. N Channel FET Sinking Current Source

In the lower left corner of Fig 1 reference Vr, op amp, N channel mosFET, and R1 form a current source. R1 connects to 'ground' via the inside Kelvin terminal of the sense resistor R0 and Vr connects to ground at its outside Kelvin terminal. The current source output current (I lower) is basically the current in the lower R1 because the mosFET gate current is nearly zero. The gate-source voltage required to turn on the FET is provided by the op amp inside a feedback loop. The op amp regulates the voltage on the top side of R1 to the fixed value Vr. The voltage on the bottom side of R1 varies with motor current. The equation for the lower, sinking, current source output (I lower) is (Vr + Im x Ro)/R1, where Im is motor current out of the leg and Ro is the sense resistor. Vr is chosen to always exceed the maximum voltage of the sense resistor (Im x Ro), therefore the current source output current just varies about a bias current without ever going to zero.

C. P Channel FET Sourcing Current Source

The top sense resistor is embedded in a current source that is similar to the current source on the bottom except that it uses a P channel mosFET to source current rather than sink it. The equation for the upper, sourcing, current source output (I upper) is (Vr - Im x Ro)/R1, where Im is motor current out of the leg.

The difference current (Iout) between the opposed upper and lower current sources is the desired signal current that tracks the motor current. Iout can directly be used as the input to the motor current A/D converter.

D. Output Equation

The output current of each current source can be separated into a nominally fixed bias current (Vr/R1) and a variable motor current (Ro/R1) x Im. When the motor has no current (Im=0), the bias current sourced by the upper current source (Vr/R1) is nominally the same as the bias current sunk by the lower current source (Vr/R1), so the offset current to the A/D is nominally zero.

In the case where the motor current (Im) is flowing from the +bus (into the top power transistor) and out of the leg, as shown by the solid arrow in Fig 1, then the amplitude of the upper sourcing current source current (I upper) is *reduced* below the bias value while the sinking current source current (I lower) remains at the bias value. The difference current, which is sunk from the A/D converter, is Iout = Ilower – Iupper = Vr/R1 - {Vr/R1 - (Ro/R1) x Im} = (Ro/R1) x Im.

In the case where the motor current (Im) is flowing from ground (into the bottom flyback diode) and out of the leg, as shown by the dotted arrow in Fig 1, then the amplitude of the upper sourcing (I upper) is at the bias value, while the sinking current (I lower) is *increased* above the bias value. The difference current, which is sunk from the A/D converter, is {Vr/R1 + (Ro/R1) x Im} - Vr/R1 = (Ro/R1) x Im, which is exactly the same as in the previous case. Thus we have demonstrated that the output current of Fig 1 is invariant to the state of the power stage.

Any shoot-though currents in the power stage are not sensed because shoot-through currents make canceling reductions in the amplitude of both the upper and lower current sources. During power stage switching transitions motor current splits between the two sense resistors so both current source currents will differ from their bias values, yet the difference output current to the A/D remains unchanged at (Ro/R1) x Im.

In summary the output current Iout of Fig 1, which is the unbalance current from opposed upper and lower current sources, accurately, rapidly, and continuously tracks the motor current amplitude and polarity with a scale factor (Ro/R1) and with (ideally) no sensitivity to the state of the inverter and (ideally) no sensitivity to +bus.

E. References

The circuit of Fig 1, however, has some architectural weaknesses that need to be addressed before a practical circuit can result. One serious weakness in Fig 1 is that upper and lower bias currents are set independently by two different references. This causes the output offset current to be sensitive in the first order to the voltage drift of both references. For output offset in Fig 1 to be stable two stable references are required.

An effective fix for this problem is to replace the independent upper reference with a slave reference that accurately tracks the lower reference. Fig 2 shows how this can be done.

A reference current source is built using the same type op amp and N channel FET used in the lower tracking current source and is driven by external reference Vr. The same value resistor is used as a load for the current source and in the source leg of the FET to set the current. The voltage across the lower R2 becomes the lower reference for the circuit, and the voltage across the upper R2, stabilized with parallel capacitor C1, becomes the upper slave reference. It does not matter that the DC impedance of the upper slave reference is not low since it will be very lightly loaded by only the non-inverting input(s) of CMOS op amps.

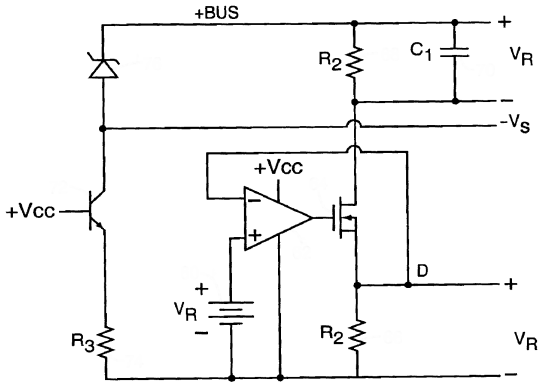

Figure 2. Slave Reference & Supply Bleed

In the configuration of Fig 2 if the external reference Vr drifts up x%, then the magnitude of the upper and lower circuit references increase x%. This means that when the circuit of Fig 2 is used to provide the references for Fig 1, drifts in the external reference Vr cause the bias currents of the upper and lower tracking current sources to drift up and down together. The output offset current, which is the difference between the upper and lower bias currents, is thus greatly desensitized to drifts in the external reference Vr, typically by two order of magnitude or more.

With Fig 2 mated to Fig 1 the need for two stable references disappears, in fact, somewhat surprisingly, *no* stable reference is now needed. The stability requirements of the required single external reference are low enough that it can be almost any available board analog reference.

F. Powering the Upper Circuitry

The left side of Fig 2 also shows a simple way to power the circuitry at the +bus. The upper op amp can just be hung from the +bus and powered by a current bled from the +bus to ground. A standard 5% zener in parallel with the op amp power terminals is adequate to regulate the supply voltage. Use of a CMOS rail-rail op amp keeps the power dissipation low and the biasing simple. A simple current source built using a high voltage NPN, emitter resistor R3, and board supply voltage +Vcc is adequate to bias the zener. For a 90 VDC design the NPN was a small surface mount package biased at a few ma.

G. Tracking A/D Converter

The output current, Iout, of Fig 1 is fed into a ground referenced tracking A/D shown in Fig 3. The A/D's quantized feedback regulates its input voltage to be near its op amp bias voltage, which is set at half the logic supply voltage (Vcc/2). With proper design this is high enough above ground to keep the sinking current source's N channel FET in the linear region, and since this voltage is near ground it means that most of the bus voltage, and most of the power dissipation, is handled by the sourcing current source's P channel FET.

The current source character of Iout makes this current sense circuit reasonably insensitive to small voltage differences between the power ground and the A/D ground, which can arise when single point grounding is used. This contributes to the practicality of the circuit.

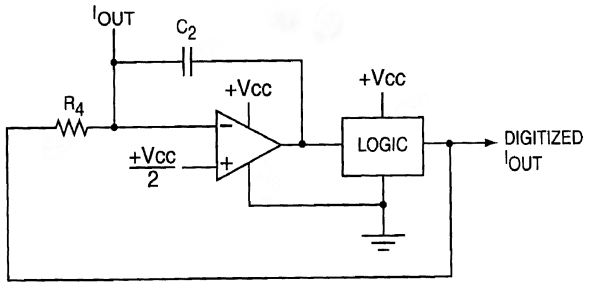

Figure 3. Tracking A/D Converter

H. Noise Filtering

A practical design requires some well placed filters. It is essential that the upper and lower tracking current sources *always* remain in the linear region, especially when a tracking A/D converter is used, otherwise the output current is badly corrupted. The necessary filtering is shown in Fig 4.

C5 to ground stabilizes the drain voltage of the lower N channel FET, and C4 to the +bus, assisted by R5, stabilizes the drain voltage of the upper P channel FET. R6 provides some isolation between the power ground and the A/D ground.

It is always good practice to low pass filter the output voltage of sense resistors since the output contains an Ldi/dt term. In addition in this current sense circuit it is desirable to soften the rise and fall time of the sense voltages so as not to excessively disturb the current loops, which have loop response times set by the op amps' bandwidth.

The sense resistor filters are the upper and lower C3 which break against the split source resistors R1. The upper and lower sense RC time constants should be set to the same value to insure that the output current to the A/D does not glitch when the power stage switches. The RC time constants of all these filters were set in the 0.5 to 1 usec range

Since these filters need to be effective at high frequencies, the placement of the caps in a surface mount layout is a critical part of the design and must be done with great care.

IV. Practical Circuit

A. Sensing Two Currents

Fig 5 shows a practical implementation for sensing two currents of a three phase servo motor. The required noise caps of Fig 4 are omitted from Fig 5 for clarity.

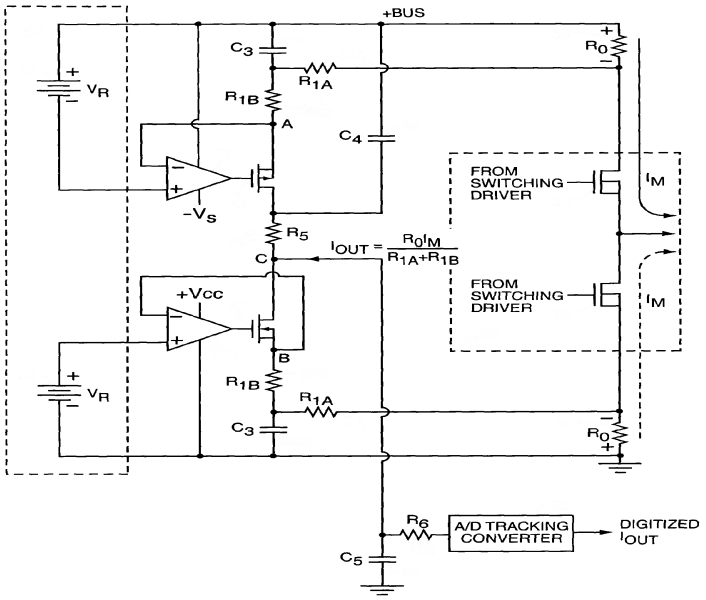

Figure 4. Location of Noise Filter Capacitors

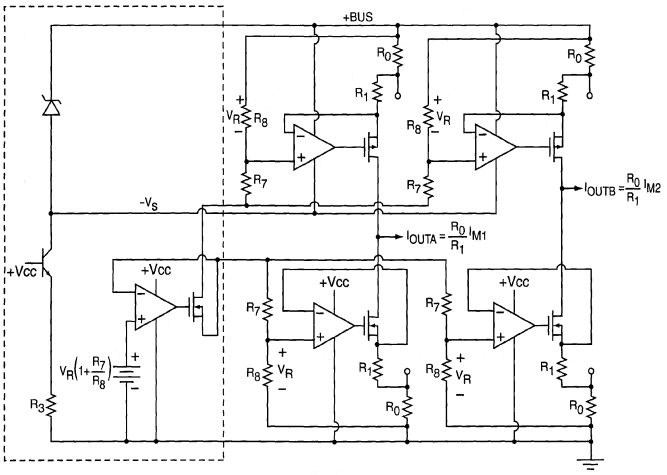

Figure 5. Sensing Two Motor Currents

B. Shared References

Fig 5 includes an additional refinement of the design. This is means to share one top/bottom reference pair between two legs. While not theoretically as good as duplicating the references for the second leg, it is considerably simpler, and when laid out carefully, it was found to work well. At the reference input of all four tracking current sources is an attenuating resistor pair (R7, R8). It serves two purposes. First, it attenuates the system board 1.5V reference to 250 mv, which is the voltage used to bias the current sources. Second, it provides each current source with a local, quasi-floated reference that can be tied to the Kelvin terminal of its sense resistor.

C. Layout Considerations

The errors associated with the fact that the references of the two legs are weakly coupled can be minimized by laying out the board so that the voltage between the electrically commoned sense resistors is small. In practice this means laying out the board so that the upper sense resistors are adjacent and the lower sense resistors are adjacent. The external reference (Vr x (1 + R7/R8)) should tie to ground at the common terminal of the bottom sense resistors.

D. Circuit Details

The design of Fig 5 uses five, small, inexpensive FET's (three N channel and two P channel) and two multiple, general purpose, CMOS, rail-rail op amp packages (a dual and a quad) for the current sources plus an NPN to power the top circuitry. Total dissipation of all the transistors at 90 VDC can be less then 600 mw. While the full design has a fair number of parts, they are mostly resistors and capacitors that pack well so the board layout area can be small. The major parts cost is the cost of the sense resistors. The offset is mostly a function of resistor tolerances and op amp voltage offsets, because these parameters control the match between the upper and lower bias currents. The op amp offset voltage and resistors should be chosen for low drift with temperature.

V. Circuit Status

This current sensor is used in a state of the art digital servo drive that has been on the market for two years. Extensive testing and production experience has shown the offset and scale factor to be quite stable. In fact the offset has been shown to be more stable than previous generations of drives and the AC drives in the same servo family. The good offset stability allows the offset to be permanently nulled at drive manufacture.

A. Patent Granted

This current sense circuit has recently been granted US patent # 6,998,800, issued Feb 14, 2006, assigned to Kollmorgen Corp. The author is listed on the patent as the sole inventor.

VI. Caveats

A. Low Bus Voltage Lockout

This current sensor does not work at very low bus voltage because both top and bottom current sources must be in the linear region for the output to be valid. This limitation for a modern digital drive is a minor one. In modern digital drives the bus voltage is normally already monitored for reasons of motor control and/or diagnostics, so a work around for this limitation is an interlock that disables the power stage when the bus voltage is below a threshold voltage. A threshold of 12V is reasonable and with design attention could probably be lower.

B. Bus Voltage Range

The circuit that was built operates from 20 VDC up to 90 VDC on the bus. The design could probably be pushed with only a small size and cost penalty to 180 VDC. The tradeoff is that as bus voltage rises so does the power dissipation and voltage rating of most of the transistors in the design. There is a fairly good selection of small surface mount transistors with a 100V rating that are inexpensive (10 to 12 cents). Small surface mount transistors with voltage ratings of 200V or 300V exist, but the selection is thinner. In a production version of this design the P channel transistors were biased at approximately 1 ma, so their dissipation was in the 100 mw range compatible with a small part.

VII. Summary

This paper has described a new current sensing circuit for a DC powered three phase servo drive of the type where the inverter and digital control electronics share a common ground. It is suitable for use in small, surface mount, single board DC powered servos. It is relatively simple and inexpensive, yet it provides continuous, highly accurate monitoring of motor currents. Its offset is very stable allowing it to be permanently nulled at drive manufacture.